REMARKS

In accordance with the foregoing claims 1-16 and 21 have been cancelled without prejudice to or disclaimer of the subject matter recited therein.

Claims 17 and 18 are pending and under consideration.

Reconsideration is respectfully requested.

I. Rejections under 35 U.S.C. §102(b)

Claims 17 and 18 stand rejected under 35 U.S.C. § 102(b) as being anticipated by JP 10-302277 ('277). This rejection is respectfully traversed.

The reference of record, '277, discloses an optical device with *a phase comparator with automatically variable frequency waveform*, which can change frequency characteristics in accordance with an **external input from** the **PLL circuit 7**. (See electronic translation page 11 paragraphs 0064 and 0066 and FIGs. 13 and 14) (Emphasis added). The '277 reference discloses that D flip flops 151 and 153 together with the NOR gates 159 and 160 are equivalent to the conventional phase comparator 26 in FIG. 2. D flip-flops 161 and 162 are adjustable monostable multivibrators which adjust a time constant based on an external input voltage level.

The Action equates element 127 and elements 161 and 164 from drawings 13 and 14, respectively, as disclosing a Phase lock loop circuit (PLL). However, as described in the machine translation at paragraph 0066 "the signal PLCK of the PLL circuit 7 (refer to drawing 1) pass to the FV converter 163," clearly indicates that element 127 is not the PLL circuit (i.e., element 7 of drawing 1). In contrast, claim 17 of the present invention recites that the PLL circuit *receives* the first clock signal not *produces* a first clock signal (PLCK) as the reference discloses. As described above, element 127 makes up the *phase comparator with automatically variable frequency waveform.* The PLL circuit is element 7 as shown in drawing 1.

The Action then equates the PLCK signal with the "first clock signal" recited in claim 17. However, as shown in FIG. 1 of the cited reference the PLL circuit 7 is not located in element 127. Rather, the PLL circuit 7 provides a clock signal PLCK to element 127 in drawing 13.

Further, the '277 reference does not disclose that the PLL circuit 7 receives any of the matrixed signals as recited in claim 17. Rather, in the '277 reference the matrixed signals (i.e., a1 and b1 in drawing 13) are never processed in the PLL circuit 7 and are processed separately from the circuit 7 as shown in the drawings 1, 13 and 14. Also, as seen in FIG. 12 the tracking error signal a5 b5 is based on the pits detected on the disc as shown by signals a2 b2.

In contrast, claim 17 recites "a phase lock loop circuit receiving a first clock signal and each matrixed signal, the phase lock loop circuit outputting second and third clock signals synchronized with the respective matrixed signals; and a phase detector which compares a phase of the second synchronized clock signal with a phase of the third synchronized clock signal to generate the tracking error signal, wherein the tracking error signal is independent of a length of pits and/or marks on the optical disk recording track."

In view of the foregoing, Applicant respectfully submits that independent claim 17 patentably define the present invention over the citations of record. Further, the dependent claim 18 should also be allowable for the same reasons as their respective base claims and further due to the additional features that they recite.

II. Conclusion

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Applicants believe that the present Amendment is responsive to each of the points raised by the Examiner in the Official Action. However, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to such matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 503333.

Respectfully submitted,

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